DEVICE APPLIED TO SCALING FACTOR OF HORIZONTAL SCAN OF A SCANNER AND METHOD THEREOF

Field of the invention

The present invention relates to a device applied to scaling factor of horizontal scan of a scanner and a method thereof. The present invention can reduce the occupied area, increase the scanning speed, and enhance the image quality of the scanner.

Background of the invention

In the realm of scanner, the scaling function is usually utilized. For instance, when a scanner having a resolution of 1200 dots per inch (dpi) is used to scan a picture having a resolution of 400 dpi, the scaling factor thereof is 1/3. Mutual coordination in the horizontal and vertical directions is required for the above scaling. If the scaling factor is 1/3, the scaling in the horizontal direction needs to be 1/3, and the scaling in the vertical direction also needs to be 1/3.

There are two kinds of manufacturing methods for the scaling in the horizontal direction, one being pixel-abstraction method, the other being pixel-average method. In the pixel-abstraction method, when a scanner scans a horizontal line, only one pixel is taken out from adjacent pixels to represent these n pixels. This method has the disadvantages of discontinuity and inferior image quality. In the pixel-average method, when a scanner scans a horizontal line, the average value of n adjacent pixels is used to represent these n pixels. This method can obtain better image quality, and has no disadvantage of discontinuity. Therefore, the pixel-average method is usually used as the manufacturing method for the scaling in the horizontal direction.

The commonly used scaling factors in the horizontal direction of a scanner are 2/3, 1/2, 1/3, 1/4, 1/6, 1/8, 1/12, and so on. The above scaling factors are all combinations of 2, 1/2 and 1/3. That is, their functions can be achieved using combinations of (2, 1/2, 1/3). For instance, when the scaling factor is 1/6, 1/2 can first be done, and then 1/3; or 1/3 can first be done, and then 1/2.

During the average process, 2 or 1/2 can easily be achieved by left-shifting 1 bit (2) or right-shifting 1 bit (1/2) the added result of pixels. However, the manufacturing of 1/3 is much more difficult. There are two commonly used methods. One is dividing the added result of pixels by 3 using a divider. This method has the disadvantages of occupying a too large area (mainly because the divider occupies a too large area) and a too slow scanning speed due to a slower processing speed of the divider.

The other commonly used method is achieving the function of dividing by 3 through referring to a table. Although this method has a faster processing speed, a read only memory (ROM) thereof will occupy a very large area. With a 16-bit scanner as an example, there will be 16×2^{16} decoders and 16×2^{16} encoders. The more the number of bits, the faster the area increases. Therefore, this method also has the disadvantage of occupying a too large area.

Accordingly, the present invention aims to propose a device applied to scaling factor of horizontal scan of a scanner and a method thereof, whereby a simpler method can be used to manufacture scaling factor of horizontal scan of a scanner, and the area occupied by the device can be effectively decreased.

Summary of the invention

The primary object of the present invention is to provide a device applied to

scaling factor of horizontal scan of a scanner and a method thereof, wherein a multiplexer, controllable shifters, and adders are used to achieve this function, hence resolving the problem of occupying a too large area in the prior art.

The secondary object of the present invention is to provide a device applied to scaling factor of horizontal scan of a scanner and a method thereof, whereby when the latency is ($\log_2 n$ - 1) clocks, the value of n is at least 2^i more than the number of bits of the scanner (i is an integer). If a pipeline architecture is matched, the scanning speed can be increased and the image quality can be enhanced.

The various objects and advantages of the present invention will be more readily understood from the following detailed description when read in conjunction with the appended drawing, in which:

Brief description of the drawings:

Fig. 1 is a block diagram of a preferred embodiment of the present invention;

Fig. 2 is a flowchart of a preferred embodiment of the present invention;

Fig. 3 is a block diagram of another preferred embodiment of the present invention; and

Fig. 4 is a flowchart of another preferred embodiment of the present invention.

Detailed description of the preferred embodiments

Fig. 1 shows a block diagram of a preferred embodiment of the present invention. In this embodiment, a digital signal is transferred to a multiplexer (MUX) 12 via an input signal 10. The multiplexer 12 is a 2-to-1 and n-bit

multiplexer. The multiplexer 12 is respectively connected to a controllable shifter 14 and an adder 16 via conducting wires. The above controllable shifter 14 is a controllable shifter capable of adjusting different shifting bits according to the numbers of bits and clocks. The controllable shifter 14 is then respectively connected to the adder 16 and an output signal 145 via conducting wires. Finally, the adder 16 is connected to the multiplexer 12 via conducting wires to be used as one input of the multiplexer 12. The above preferred embodiment applies to input signals with the number of bits between (2^3+1) and 2^4.

Fig. 2 shows a flowchart of a preferred embodiment of the present invention. The present invention comprises mainly the following steps.

An input signal 20 with clock 0: The selected signal of a multiplexer 22 is a signal outputted from the input signal 20. The number of bits of the input signal 20 is between 2^3+1 and 2^4. A controllable shifter 24 judges the shifting bits to right-shift the output signal of the selected signal of the multiplexer 22 two bits. An adder 26 adds the output signal shifted the judged number of bits by the controllable shifter 24 and the output signal of the selected signal of the multiplexer 22.

The input signal 20 with clock 1: The selected signal of the multiplexer 22 is the added output signal of the adder 26. The controllable shifter 24 judges the shifting bits to right-shift the output signal of the selected signal of the multiplexer 22 four bits. The adder 26 adds the output signal shifted the judged number of bits by the controllable shifter 24 and the output signal of the selected signal of the multiplexer 22.

The input signal 20 with clock 2: The selected signal of the multiplexer 22 is the added output signal of the adder 26. The controllable shifter 24 judges the shifting bits to right-shift the output signal of the selected signal of the multiplexer 22 eight bits. The adder 26 adds the output signal shifted the judged number of bits by the controllable shifter 24 and the output signal of the selected signal of the multiplexer 22.

An input signal 20 with clock 3: The selected signal of the multiplexer 22 is the added output signal of the adder 26. The controllable shifter 24 judges the shifting bits to right-shift the output signal of the selected signal of the multiplexer 22 two bits, and then outputs to an output signal 28.

Scaling factor of horizontal scan of a scanner can thus be achieved without the need of a divider and a ROM occupying a too large area in the prior art, thereby effectively decreasing the occupied area of the device, simplifying the manufacturing process, increasing the scanning speed, and enhancing the image quality of the scanner.

Fig. 3 shows a block diagram of another preferred embodiment of the present invention. In this embodiment, a digital signal is transferred to a first adder 102 and a first shifter 104 via an input signal 100. The number of bits of the digital signal is between 2^3+1 and 2^4. The first shifter 104 is connected to the first adder 102 via conducting wires. The first adder 102 is then connected to a second adder 106 and a second shifter 108 via conducting wires. The second shifter 108 is connected to the second adder 106 via conducting wires. Next, the second adder 106 is connected to a third adder 110 and a third shifter 112 via conducting wires. The third shifter 112 is connected to the third adder

110 via conducting wires. Subsequently, the third adder 110 is connected to a fourth shifter 114 via conducting wires. Finally, the fourth shifter 114 is connected to an output signal 116.

Fig. 4 shows a flowchart of another preferred embodiment of the present invention. The present invention comprises mainly the following steps.

First, an input signal 200 outputs signals to a first adder 204 for addition and a first shifter 202 to be right-shifted 2 bits. The number of bits of the input signal 200 is between 2^3+1 and 2^4. After the first shifter 202 right-shifts 2 bits, the output signal is transferred to the first adder 204 for addition.

The first adder 204 adds the input signal 200 and the output signal right-shifted 2 bits by the first shifter 202, and outputs the output signal to a second adder 208 for addition and a second shifter 206 to be right-shifted 4 bits. After the second shifter 206 right-shifts 4 bits, the output signal is transferred to the second adder 208 for addition.

The second adder 208 adds the output signal of the first adder 204 and the output signal right-shifted 4 bits by the second shifter 206, and outputs the output signal to a third adder 212 for addition and a third shifter 210 to be right-shifted 8 bits. After the third shifter 210 right-shifts 8 bits, the output signal is transferred to the third adder 212 for addition.

The third adder 212 adds the output signal of the second adder 208 and the output signal right-shifted 8 bits by the third shifter 210, and outputs the output signal to a fourth shifter 214 to be right-shifted 2 bits.

After the fourth shifter 214 right-shifts 2 bits, the output signal is transferred to an output signal 216.

Scaling factor of 1/3 of horizontal scan of a scanner can thus be achieved without the disadvantage of occupying a too large area by the device in the prior art. Because all the above four shifters are fixed right-shift type, there can be no logical gates in practice. Therefore, the device will not occupy a too large area, and the cost will not be increased. Additionally, the two inputs of each of the above three adders are related. For instance, one input (input 1) of the first adder is A, the other input (input 2) thereof will be 1/4 A. Adders having inputs thus related can be much simplified. The area thus will not be enlarged. Another advantage of this method is that when a faster latency is required, or there is no pipeline architecture, this method can also be used to achieve the scaling factor of 1/3 of horizontal scan of a scanner.

The above two manufacturing methods in Figs. 2 and 4 can be used to achieve the scaling factor of 1/3 of horizontal scan of a scanner. The principle is as follows with a signal A of 16 bits as an example.

Right-shifting n bits represents dividing a signal by 2^n. Therefore, Fig. 2 and Fig. 4 are functions for calculating $(A+A/2^2)\cdot(1+1/2^4)\cdot(1+1/2^8)\cdot 1/2^2$.

$(A+A/2^2)\cdot(1+1/2^4)\cdot(1+1/2^8)\cdot 1/2^2$

$=A\cdot 1/2^2\cdot(1+1/2^2)\cdot(1+1/2^4)\cdot(1+1/2^8)$

$=A/4\cdot(1+1/2^2+1/2^4+1/2^6+1/2^8+1/2^{10}+1/2^{12}+1/2^{14})$

$=A/4\cdot(1+1/2^2+1/2^4+1/2^6+1/2^8+1/2^{10}+1/2^{12}+1/2^{14}+1/2^{16}+1/2^{18}+\ldots)$ ($A/2^n=0$ if $n\geq 16$)

$=1/3\ A$

Thus, the above two methods are used to achieve the scaling factor of 1/3 of horizontal scan of a scanner. Said embodiments use the device composed of

single adder and shifter or composed of three adders and four shifters to achieving the function of calculating the scaling factor of horizontal scan. Furthermore, the present invention could also use at least an adder and a shifter to achieving the function of calculating the scaling factor of horizontal scan. In other word, if only it uses the technology principle of the present invention, it would belong to the embodiments of the invention that no matter how many the adder and the shifter are used. Said embodiments are intended to be embraced within the scope of the invention as defined in the appended claims.

To sum up, the present invention relates to a scanner and, more particularly, to a device applied to scaling factor of horizontal scan of a scanner and a method thereof. The present invention can reduce the occupied area, increase the scanning speed, and enhance the image quality of the scanner.

Although the present invention has been described with reference to the preferred embodiment thereof, it will be understood that the invention is not limited to the details thereof. Various substitutions and modifications have been suggested in the foregoing description, and other will occur to those of ordinary skill in the art. Therefore, all such substitutions and modifications are intended to be embraced within the scope of the invention as defined in the appended claims.